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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,383	09/15/2004	Timothy H. Daubenspeck	BUR920040151US1	5382

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EXAMINER	
DANG, TRUNG Q	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,383	DAUBENSPECK ET AL.	
	Examiner	Art Unit	
	Trung Dang	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *15-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 7 and 12-14* is/are rejected.

7)☒ Claim(s) *6 and 8-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, 7 and 12-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Ference et al. of record.

With reference to the first embodiment illustrated in Figs. 4-8, the prior art anticipates the claimed invention in that it discloses a method for chip separation comprising the steps of:

(a) providing a semiconductor substrate;

(b) forming first and second device regions 12a, 12b and a filled deep trench 18 in and at top of the semiconductor substrate,

wherein the first and second device regions 12a, 12b are separated by a semiconductor border region 14 of the semiconductor substrate, and

wherein the semiconductor border region 14 comprises the filled deep trench 18 (Fig. 4);

(c) forming N interconnect layers 22, in turn, directly above the border region 14 and the first and second device regions 12a/12b,

wherein N is a positive integer greater than one (*Fig.5 and col.5, lines 2-10. Note that, lines 7-10 discloses that "for some applications additional intermediate conductive layers may be used in which other wiring and/or contact vias are formed in the edge connection area." Thus, depending on a particular application, interconnect layer 22 includes additional intermediate conductive layers, therefore the composite interconnect layer 22 consists of the interconnect layer 22 and the additional intermediate conductive layers reads on the claimed limitation recited at step (c), wherein N is a positive integer greater than one*),

wherein each layer of the N interconnect layers 22 comprises an etchable portion (*portion of the composite interconnect layer 22 that is removed in subsequent step depicted in Fig.6B*) directly above the filled deep trench 14, and

wherein the etchable portions of the N interconnect layers form a continuous etchable block directly above the filled deep trench 14 (*or above the semiconductor border region 14 as claimed in claim 1. See Fig. 6A*), and

wherein the entire continuous etchable block comprises essentially a same material (*the removed portion of the composite interconnect layer 22 comprises essentially a same material, e.g., metallic material*);

(d) removing the continuous etchable block by etching (*Fig. 6B and col. 5, lines 27-29*); and

(e) cutting with a laser through the filled deep trench via an empty space of the removed continuous etchable block (*line 64 of col. 5 to line 6 of col. 6*).

Note that, the terms deep and shallow are relative to the extent of being definitive only in regard to a particular object referred to, hence the filled shallow trench 18 of the reference reads on the claimed filled deep trench.

For claim 3, see col. 4, line 67 for the composite interconnect layer 22, and hence the continuous etchable bock comprises copper.

For claim 7, see Fig. 14 of the second embodiment, wherein the etching of the continuous etchable block is performed until a surface of the semiconductor border region 114 is exposed to the atmosphere.

3. Claims 1 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Takao of record.

With reference to Figs. 5-8B, the reference teaches the claimed invention in that it discloses method for chip separation comprising the steps of:

(a) providing a semiconductor substrate 10,

(b) forming first and second device regions 10A (Fig. 8B) in and at top of the semiconductor substrate 10, wherein the first and second device regions are separated by a semiconductor border region of the semiconductor substrate 10

(*Fig. 8A wherein the dicing line region corresponds to the claimed semiconductor border region*)

(c) forming N interconnect layers, in turn, including a bottom copper layer 21 and a top barrier metal layer (not shown in Fig. 5) directly above the semiconductor border region and the first and second device regions 10A using photoresist layer 19 as a mask (Fig. 5 and paras. [0061]-[0063]),

wherein N is a positive integer greater than one,

wherein each layer of the N interconnect layers comprises an etchable portion (*photoresist block 19 reads on this limitation because the photoresist block 19 connects the left and right portions of the bottom copper layer 21 and the top barrier layer. That is, the photoresist block 19 is considered as an integral part of the two metal layers*) directly above the semiconductor border region, and wherein the etchable portions of the N interconnect layers form a continuous etchable block directly above the semiconductor border region, and wherein the entire continuous etchable block 19 comprises essentially a same material;

(d) removing the continuous etchable block by etching (Fig. 7 and para. [0064];

(e) cutting with a laser through the semiconductor border region via an empty space of the removed continuous etchable block (Fig. 8B and para. [0066]).

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takao as above in view of Chae et al. (US 6,958,312).

Takao teaches a method for chip separation as described above.

Takao differs from the claims in not disclosing that the photoresist block is removed by wet etching.

Chae recognizes that it is known to remove a photoresist mask using a wet etching process. However, the conventional solvents causes metal line formed of copper easily corroded (col. 2, lines 15-20). Accordingly, Chae teaches a solvent composition which is used to remove the photoresist material without corroding copper metal line (col. 2, lines 37-40; col. 3, lines 64-67).

It would have been obvious to one of ordinary skill in the art to modify Takao's teaching by removing the photoresist block 19 using a wet etching process with the solvent composition taught by Chae because the use of such solvent would prevent corrosion of the copper interconnect layer 21.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ference as above in view of Kawakami of record.

Ference teaches a method for chip separation as described above.

Ference differs from the claim in not disclosing the steps of backside grinding and then applying a dicing tape as claimed.

Kawakami teaches a chip separation method, which includes the steps of: backside grinding a back surface of a semiconductor wafer; and then affixing a dicing tape to the back surface of the semiconductor substrate before dicing the substrate (Fig. 2 and paras. [0054]-[0056]).

It would have been obvious to one of ordinary skill in the art to modify Ference's process by performing a backside grinding process and affixing a dicing tape to the back surface of the semiconductor substrate as suggested by Kawakami because of the following benefits: a) thinning the substrate would produce extremely thin chip or die, hence increasing the capacity of chips stacked on top of each other for a given dimension, and b) the dicing tape affixed to the backside of the substrate not only provides support for the dicing operation but also facilitates handling of the chips after they are separated.

Allowable Subject Matter

7. Claims 6 and 8-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

Claim 6 is allowable over prior art of record because the prior art does not teach or suggest the claimed subject matter which includes the step of wet etching a portion of the semiconductor border so as to form a v-shaped trench after the step of removing the etchable block but before the step of cutting by laser.

Claim 8 and its dependent claims are allowable over prior art of record because the prior art does not teach or suggest the claimed subject matter which includes the claimed feature regarding the formation of the first and second chip edge blocks, the first and second isolation blocks, and their positions with respect to each other as recited in claim 8.

Response to Arguments

9. Applicant's arguments with respect to claims 1 and 12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. This application contains claims 15-20 drawn to an invention nonelected with traverse in Paper No. 06/06/05. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Dang whose telephone number is 571-272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trung Dang
Primary Examiner
Art Unit 2823

12/08/05